IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 1, 5 and 8 and ADD new claims 11 and 12 as follows:

1. (currently amended) A circuit, comprising:

a register which stores therein a semaphore address; and

a semaphore control circuit which asserts a control signal in response to a read access by a processor directed to the semaphore address, and negates the control signal in response to a write access by the processor directed to the semaphore address,

wherein other resources are prohibited from accessing the semaphore address when the control signal is asserted.

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2. (original) The circuit as claimed in claim 1, further comprising a comparator which makes a comparison of an address output from the processor with the semaphore address stored in said register, and asserts a match signal when the comparison indicates a match, wherein said semaphore control circuit includes:

a circuit which sets the control signal to an asserted state in response to assertion of the match signal and an indication of a read operation by a read/write signal output from the processor; and

a circuit which resets the control signal to a negated state in response to the assertion of the match signal and an indication of a write operation by the read/write signal output from the processor.

3. (original) The circuit as claimed in claim 1, wherein a right to use a bus given to the processor is not relinquished in response to a bus-arbitration request supplied from an external source during an asserted state of the control signal.

4. (original) The circuit as claimed in claim 3, further comprising a bus-arbitration control circuit which receives a signal indicative of the bus-arbitration request, the control signal, and a chip enable signal output from the processor, said bus-arbitration control circuit operating not to assert a bus-arbitration-acknowledge signal in response to the bus-arbitration request signal regardless of a state of the chip enable signal if the control signal is in an asserted state, operating not to assert the bus-arbitration-acknowledge signal in response to the bus-arbitration request signal if the chip enable signal is in an asserted state and the control signal is in a negated state, and operating to assert the bus-arbitration-acknowledge signal in response to the bus-arbitration request signal if the chip enable signal is in a negated state and the control signal is in the negated state.

5. (currently amended) A processor, comprising:

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a processor core;

a register which stores therein a semaphore address; and

a control circuit which asserts a control signal in response to a read access by said processor core directed to the semaphore address, and negates the control signal in response to a write access by said processor core directed to the semaphore address,

wherein other resources are prohibited from accessing the semaphore address when the control signal is asserted.

6. (original) The processor as claimed in claim 5, wherein said control circuit includes:

a comparator which makes a comparison of an address output from said processor core with the semaphore address stored in said register, and asserts a match signal when the comparison indicates a match;

a circuit which sets the control signal to an asserted state in response to assertion of the match signal and an indication of a read operation by a read/write signal output from said processor core; and

a circuit which resets the control signal to a negated state in response to the assertion of the match signal and an indication of a write operation by the read/write signal output from said processor core.

7. (original) The processor as claimed in claim 5, wherein a right to use a bus is not relinquished in response to a bus-arbitration request supplied from an external source during an asserted state of the control signal.

8. (currently amended) A multi-processor system, comprising:

a plurality of processors;

a memory shared by said plurality of processors; and

a semaphore register for controlling exclusive use of said memory, wherein at least one of said plurality of processors includes:

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a processor core;

an address register which stores therein an address of said semaphore register; and

a control circuit which asserts a control signal in response to a read access by said processor core directed to the address stored in said address register, and negates the control signal in response to a write access by said processor core directed to the address stored in said address resister,

wherein other resources are prohibited from accessing the semaphore address when the control signal is asserted.

9. (original) The multi-processor system as claimed in claim 8, wherein said control circuit includes:

a comparator which makes a comparison of an address output from said processor core with the semaphore address stored in said address register, and asserts a match signal when the comparison indicates a match;

a circuit which sets the control signal to an asserted state in response to assertion of the match signal and an indication of a read operation by a read/write signal output from said processor core; and

a circuit which resets the control signal to a negated state in response to the assertion of the match signal and an indication of a write operation by the read/write signal output from said processor core.

10. (original) The multi-processor system as claimed in claim 8, wherein said at least one of said plurality of processors does not relinquish a right to use a bus in response to a bus-arbitration request made by another one of the processors during an asserted state of the control signal.

11. (new) A method for controlling a semaphore in a system including at least one processor, comprising:

asserting a control signal when the processor performs a read access to a semaphore address; and

negating the control signal when the processor performs a write access to the semaphore address.

12. (new) A circuit, comprising:

a register storing a semaphore address; and

a semaphore control circuit which asserts a control signal in response to a read access by a processor directed to the semaphore address, and negates the control signal in response to a write access by the processor directed to the semaphore address, the control signal preventing other processors from accessing the semaphore address.